REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 19-23, and 93-118 were pending and rejected. In this response, claim 106 is canceled. Claims 19, 93, and 101 have been amended to particularly point out and distinctly claim, in full, clear, concise, and exact terms, the subject matter which Applicant regards as his invention. No new matter has been added. Continued examination of the present claims in light of the aforementioned amendments and the following remarks is earnestly requested.

Rejections under 35 U.S.C. § 102

Claims 19-23, 93-106, and 109-118 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,115,812 of Abdallah et al. (hereinafter "Abdallah").

In view of the foregoing amendments, it is respectfully submitted that claims 19-23, 93-105, and 109-118 as amended, include limitations that are not disclosed by Abdallah. Claim 19, as amended, recites:

19. A method comprising:

storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations **in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations**; and

duplicating bits from the plurality of non-contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations. (emphasis added)

Applicant respectfully asserts that Abdallah does not disclose "**in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations**", as claimed by Applicant. Referring to Abdallah (col. 6, line 44-55), the instruction SHUFPS, as disclosed, moves source data having data items A, B, C, and D into a destination register, with possibilities to occupy any location of a result data item (col.6, line 49-50). The instruction therefore needs one operand (provided by the programmer) to designate the order of data items (A, B, C, and D) when stored in the destination register. Persons having ordinary skilled in the art know that a computer instruction always returns a definite and expected result. When writing program, programmers provide sufficient operands in a computer instruction for a computer to operate on. In this case, the instruction SHUFPS, although not disclosed explicitly, receives at least one code indicating an operand to designate the locations for each data items to be shuffled into.

In addition to that, Abdallah merely moves source data into the destination register into contiguous locations and does not then duplicate the data moved into the contiguous locations, as claimed by applicant.

For at least the foregoing reasons, Abdallah fails to disclose that which applicant has claimed. Applicant believes that the claim is patentable. Applicant respectfully requests the withdrawal of the rejection for the claim 19. Moreover, dependent claims 20-23 depend from

independent claim 19. Applicant believes that claim 19 is allowable such that claims 20-23 depending there from with additional limitations are also in condition for allowance.

Similarly, independent claims 93, 101, 110, 113, and 116 include substantially the same limitation, i. e., "in response to execution of a first instruction that does not specify an order in which the plurality of non-contiguous groups of source bits are to be stored into the plurality of non-contiguous groups of destination storage locations". Thus, for the reasons similar to those discussed above, it is respectfully submitted that claims 93, 101, 110, 113 and 116 are not anticipated by Abdallah. Given that the rest of the claims depend from one of the above independent claims, it is respectfully submitted that the rest of the claims are not anticipated by Abdallah. Accordingly, Applicant respectfully submits that claims 93-105, 109-118 are patentable over the cited reference, and respectfully requests the rejections of claims under 35 U.S.C. §102(b) be withdrawn.

Claims 19, 20, 22, 93, 98, 99, 100, 101, 106 and 109 are rejected under 35 U.S.C. §102(b) as being anticipated by Sidwell et al., European Patent Application EP 9743594 Al (hereinafter "Sidwell"). Sidwell describes instructions that are used for effecting matrix transposition operations (see Abstract).

The Office Action alleges claim 19 is anticipated by Sidwell with reference to instruction "zip2n4v2p" in Figure 17. Applicant would like to point out that, Figure 17 as shown in Sidwell contains typo errors that results in misinterpretation of its meaning. Referring to definition of the instruction "zip2n4v2p" in Figure 7, the "zip2n4v2p" instruction takes two operands, "7/6/5/4" and "3/2/1/0" and moves the data elements into two destination registers. The resultant data is presented as "7/3/6/2" and "5/1/4/0". Now, referring to Figure

17, the instruction "zip2n4v2p" shows only one source operand ("V3/V2/V1/V0"), but the definition of the instruction implies an instruction "zip2n4gv2p" requires two source operands. Therefore, what is disclosed in Figure 17 is in fact the "zip2n4v2p" instruction operating on two identical source operands, "V3/V2/V1/V0". Furthermore, as a result of the instruction, figure 17 shows two destination registers storing data elements "V3/V3/V1/V1" (at left destination register) and "V2/V2/V1/V1" (at right destination register). The result is incorrect. The correct result according to the definition of the instruction in Figure 7 should return "V3/V3/V2/V2" at the left destination register and "V1/V1/V0/V0" at the right destination register. This interpretation is further established by tracing the arrows drawn in Figure 17. The arrows show that data element "V2" is directed to the second location and the first location in the left destination register (but the contents of the locations have been erroneously labeled as "V1"). The arrows also show that data element "V1" is directed to the third location and the fourth location in the right destination register (but the contents of the locations have been erroneously labeled as "V2"). The sequence of operations shown in Figure 17 can also be found in Annex B, Sequence (i) of Sidwell (page 14).

In short, Sidwell disclose an instruction "zip2n4v2p" requires two source operands, the instruction moves data elements from the source operands into two destination registers according to the pattern defined in Figure 7. The instruction moves each and every data elements in the contiguous source operands into destination registers. Sidwell does not disclose "storing a plurality of non-contiguous groups of source bits into a plurality of non-contiguous groups of destination storage locations". More importantly, Sidwell discloses all data elements in source operands are moves into destination registers (nothing more and nothing less). There is certainly no duplication or replication in the execution of the instruction. Hence, Sidwell fails to disclose "duplicating bits from the plurality of non-

contiguous groups of destination storage locations into groups of destination storage locations adjacent to the non-contiguous groups of destination storage locations".

The example described in the Office Action (using Figure 17) is fallacious because the example has been misconstrued by the typo error explained above. Using the correct definition of instruction "zip2n4v2p", the instruction does not teach the limitations as recited in Claim 19. Even assuming that there is no misprint error, the Office Action has erred in interpreting the source register shown in Figure 17 as one single operand, which in fact, the instruction requires two source operands. What is depicted in Figure 17 is about moving each and every data elements from two source operands (having same contents) into two destination registers. Again, Applicant would like to point out that no duplication and replication is involved.

For at least the foregoing reasons, Sidwell fails to disclose that which applicant has claimed. Applicant believes that the claim is patentable. Applicant respectfully requests the withdrawal of the rejection for the claim 19. Moreover, dependent claims 20 and 22 depend from independent claim 19. Applicant believes that claim 19 is allowable such that claims 20 and 22 depending there from with additional limitations are also in condition for allowance.

Similarly, independent claims 93 and 101 were rejected using the same example in the Office Action. The detailed remarks with respect to independent claim 19 are incorporated here by reference. For the reasons similar to those discussed above, it is respectfully submitted that claims 93 and 101 are not anticipated by Sidwell. Given that the rest of the claims depend from one of the above independent claims, it is respectfully submitted that the rest of the claims are not anticipated by Sidwell. Accordingly, Applicant respectfully submits that claims 93, 98, 99, 100, 101, and 109 are patentable over the cited reference, and respectfully requests the rejections of claims under 35 U.S.C. §102(b) be withdrawn.

Rejections under 35 U.S.C. § 103

Claims 107 and 108, depending indirectly on claim 101, are rejected under 35 U.S.C. 103(a) as being unpatentable over Abdallah. As presented above in remarks regarding the 35 U.S.C rejections of independent claim 101, Abdallah does not teach or suggest each and every limitation of independent claim 101. No other reference was cited by the Examiner to cure those deficiencies of Abdallah. Thus claims 107 and 108, which depend from claim 101, are patentable over Abdallah. Accordingly, Applicant respectfully request that the 35 U.S.C. §103(a) rejection of claims be withdrawn.

Claims 21, 23, 94-97, 102-105, 107, and 108 depending indirectly on independent claim 19, 93, and 101, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sidwell. As presented above in traversing the 35 U.S.C rejections of the independent claim 19, Sidwell does not teach or suggest each and every limitation of independent claims 19, 93, and 101. No other reference was cited by the Examiner to cure those deficiencies of Sidwell. Thus, claims 21, 23, 94-97, 102-105, 107, and 108, which depend from the above independent claims, are patentable over Sidwell. Accordingly, Applicant respectfully request that the 35 U.S.C. §103(a) rejection of claims be withdrawn.

CONCLUSION

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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